****

**FUNDAMENDTAL OF DIGITAL SYSTEM FINAL PROJECT REPORT**

**DEPARTMENT OF ELECTRICAL ENGINEERING**

**UNIVERSITAS INDONESIA**

**Data Compressor Circuit**

**GROUP B7**

**GROUP MEMBER 1 Ahmad Rifqi**

**GROUP MEMBER 2 Michael Winston Tjahaja**

**GROUP MEMBER 3 Laode Alif Masum**

**GROUP MEMBER 4 Mochammad Dyenta**

**PREFACE**

Everything within this project was made with the main cause of the need to pass a class. However, this was not the only goal we had in mind when making this report. We, as in everyone who partook in the creation of our project wished to further extend their abilities and see just how far we’ve gotten (skill wise) within the subject, Digital System Design, after an entire semester of learning said subject.

The design we had made for this final project is the very culmination of our combined skills being placed together into one and birthing a result that we, the practitioners are quite proud of. Hopefully this report will also be used in the near future to help other people grow and exceed in the subject as well.

Depok, December 07, 2022

Group B7

TABLE OF CONTENTS

**CHAPTER 1: INRODUCTION1**

1.1 Background2

1.2 Project Description2

1.3 Objectives2

1.4 Roles and Responsibilities2

**CHAPTER 2: IMPLEMENTATION4**

2.1 Equipment5

2.2 Implementation5

**CHAPTER 3: TESTING AND ANALYSIS4**

3.1 Testing5

3.2 Result5

3.3 Analysis5

**CHAPTER 4: CONCLUSION4**

**REFERENCES4**

**APPENDICES4**

Appendix A: Project Schematic5

Appendix B: Documentation5

# CHAPTER 1

# INTRODUCTION

## BACKGROUND

Data bits usually has a lot of the same parts which means that it is commonly repeated over and over when transmitting data. We wanted to see if we could somehow make one data that is used to be transmitted at a given frequency as to make things more efficient and cause less errors since the traditional way of creating data and then sending data then doing the whole process all over again feels very inefficient overall.

That’s when we got the idea to make a Data Compressor Circuit, tasked to be able to achieve what we wanted to make to complete this final project.

* 1. **PROJECT DESCRIPTION**

This program we made has 2 main functions which are to repeatedly count upwards if receiving the same type of data bit combination, and then resetting when it receives a different type of data bit combination.

It works by increasing a counter whenever the program receives the exact same formula of a certain string and will continue to increase the counter and transmit said data depending on how many are needed (based on the counter). The program will then completely reset whenever there is a change in the data string that is placed into the input side of the program. The counter will also reset to 0 because of this and start counting upwards again when it starts to receive the same type of data string that made it to reset.

## OBJECTIVES

The objectives of this project are as follows:

1. To reduce the size of data that is passed through a network
2. To increase the success rate transmission of data
3. To make the process of transmitting data more efficient

## ROLES AND RESPONSIBILITIES

The roles and responsibilities assigned to the group members are as follows:

|  |  |  |
| --- | --- | --- |
| Roles | Responsibilities | Person |
| Role 1 | Main Coding of the project | Ahmad Rifqi, Laode Alif Masum, Michael Winston Tjahaja |
| Role 2 | Test Bench Creation | Ahmad Rifqi, Laode Alif Masum |
| Role 3 | ModelSim Simulation | Michael Winston Tjahaja |
| Role 4 | Report | Michael Winston Tjahaja, Ahmad Rifqi |
| Role 5 | Quartus Prime Model | Ahmad Rifqi |

Table 1. Roles and Responsibilities

# CHAPTER 2

# IMPLEMENTATION

## 2.1 EQUIPMENT

The tools that are going to be used in this project are as follows:

* VSCode
* ModelSim – Intel FPGA Starter Edition Model (Quartus Prime 20.1)
* Microsoft Word
* Quartus Prime 21.1

## 2.2 IMPLEMENTATION

Lorem ipsum dolor sit amet, consectetur adipiscing elit. Morbi ornare accumsan nisl sit amet sodales. Suspendisse sed dictum velit, in suscipit sem. Vestibulum egestas neque vel velit tristique, id venenatis nunc fringilla. Mauris condimentum diam consequat egestas tincidunt. Class aptent taciti sociosqu ad litora torquent per conubia nostra, per inceptos himenaeos. Vivamus semper pharetra commodo. Integer hendrerit ultricies lacus. Nullam id magna sed risus placerat luctus sed at mauris. Curabitur ligula urna, pharetra eget mi sit amet, sagittis feugiat magna. Curabitur ex nisl, eleifend et mattis sit amet, condimentum non nisi.

Donec at iaculis leo. Integer congue sed lacus suscipit iaculis. Nulla a augue ut sapien rutrum consectetur. Sed ac dignissim lorem. Maecenas hendrerit nisl a metus posuere, vel vehicula metus eleifend. Mauris blandit, dolor nec malesuada tempor, purus nibh aliquet nibh, at faucibus leo felis a nisi. Donec pharetra leo risus, in vestibulum dui laoreet in. Nulla facilisi. Etiam nec consequat justo. Lorem ipsum dolor sit amet, consectetur adipiscing elit. Aliquam erat volutpat. Etiam pharetra eleifend hendrerit.

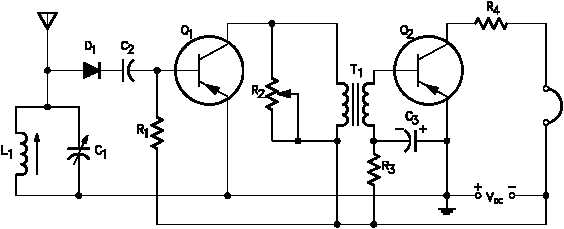


Fig 1. Schematic

Maecenas ultrices ac felis et faucibus. Suspendisse cursus eget neque non tempus. Integer id nunc blandit, mollis risus ut, rhoncus erat. Donec eleifend porttitor justo, ut suscipit ipsum fermentum eget. Proin lacinia erat et cursus suscipit. Morbi ut neque sit amet magna posuere tempor sed at urna. Ut at faucibus libero. Sed ut massa dui. In sit amet dolor fermentum, condimentum lorem interdum, aliquam metus. Aenean tincidunt elit et mollis consectetur. Nam a elit et leo vulputate gravida convallis sed lacus.

# CHAPTER 3

# TESTING AND ANALYSIS

## 3.1 TESTING

## 3.2 RESULT

Lorem ipsum dolor sit amet, consectetur adipiscing elit. Morbi ornare accumsan nisl sit amet sodales. Suspendisse sed dictum velit, in suscipit sem. Vestibulum egestas neque vel velit tristique, id venenatis nunc fringilla. Mauris condimentum diam consequat egestas tincidunt. Class aptent taciti sociosqu ad litora torquent per conubia nostra, per inceptos himenaeos. Vivamus semper pharetra commodo. Integer hendrerit ultricies lacus. Nullam id magna sed risus placerat luctus sed at mauris. Curabitur ligula urna, pharetra eget mi sit amet, sagittis feugiat magna. Curabitur ex nisl, eleifend et mattis sit amet, condimentum nonnisi.

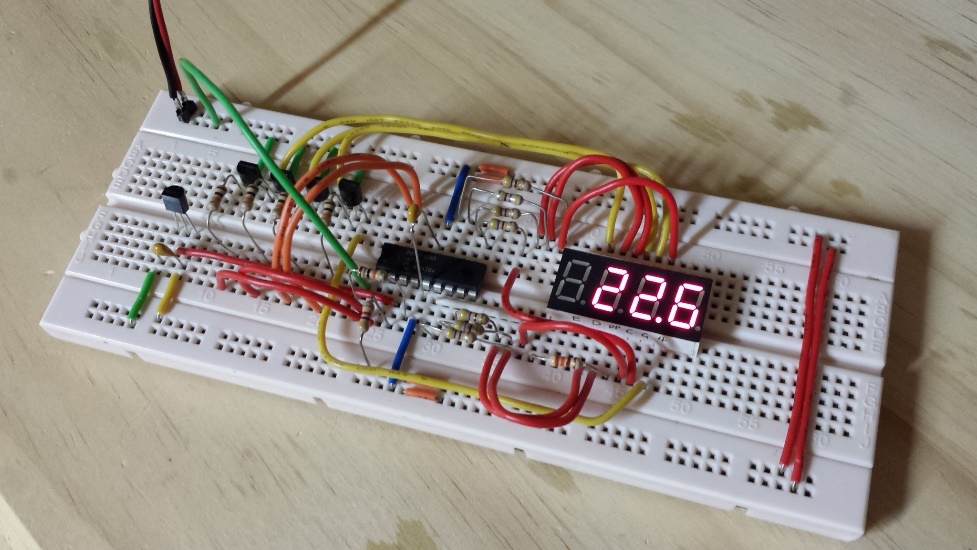


Fig 2. Testing Result

Donec at iaculis leo. Integer congue sed lacus suscipit iaculis. Nulla a augue ut sapien rutrum consectetur. Sed ac dignissim lorem. Maecenas hendrerit nisl a metus posuere, vel vehicula metus eleifend. Mauris blandit, dolor nec malesuada tempor, purus nibh aliquet nibh, at faucibus leo felis a nisi. Donec pharetra leo risus, in vestibulum dui laoreet in. Nulla facilisi. Etiam nec consequat justo. Lorem ipsum dolor sit amet, consectetur adipiscing elit. Aliquam erat volutpat. Etiam pharetra eleifend hendrerit.

## 3.3 ANALYSIS

Lorem ipsum dolor sit amet, consectetur adipiscing elit. Morbi ornare accumsan nisl sit amet sodales. Suspendisse sed dictum velit, in suscipit sem. Vestibulum egestas neque vel velit tristique, id venenatis nunc fringilla. Mauris condimentum diam consequat egestas tincidunt. Class aptent taciti sociosqu ad litora torquent per conubia nostra, per inceptos himenaeos. Vivamus semper pharetra commodo. Integer hendrerit ultricies lacus. Nullam id magna sed risus placerat luctus sed at mauris. Curabitur ligula urna, pharetra eget mi sit amet, sagittis feugiat magna. Curabitur ex nisl, eleifend et mattis sit amet, condimentum non nisi.

Donec at iaculis leo. Integer congue sed lacus suscipit iaculis. Nulla a augue ut sapien rutrum consectetur. Sed ac dignissim lorem. Maecenas hendrerit nisl a metus posuere, vel vehicula metus eleifend. Mauris blandit, dolor nec malesuada tempor, purus nibh aliquet nibh, at faucibus leo felis a nisi. Donec pharetra leo risus, in vestibulum dui laoreet in. Nulla facilisi. Etiam nec consequat justo. Lorem ipsum dolor sit amet, consectetur adipiscing elit. Aliquam erat volutpat. Etiam pharetra eleifend hendrerit.

# CHAPTER 4

# CONCLUSION

Lorem ipsum dolor sit amet, consectetur adipiscing elit. Morbi ornare accumsan nisl sit amet sodales. Suspendisse sed dictum velit, in suscipit sem. Vestibulum egestas neque vel velit tristique, id venenatis nunc fringilla. Mauris condimentum diam consequat egestas tincidunt. Class aptent taciti sociosqu ad litora torquent per conubia nostra, per inceptos himenaeos. Vivamus semper pharetra commodo. Integer hendrerit ultricies lacus. Nullam id magna sed risus placerat luctus sed at mauris. Curabitur ligula urna, pharetra eget mi sit amet, sagittis feugiat magna. Curabitur ex nisl, eleifend et mattis sit amet, condimentum non nisi.

Donec at iaculis leo. Integer congue sed lacus suscipit iaculis. Nulla a augue ut sapien rutrum consectetur. Sed ac dignissim lorem. Maecenas hendrerit nisl a metus posuere, vel vehicula metus eleifend. Mauris blandit, dolor nec malesuada tempor, purus nibh aliquet nibh, at faucibus leo felis a nisi. Donec pharetra leo risus, in vestibulum dui laoreet in. Nulla facilisi. Etiam nec consequat justo. Lorem ipsum dolor sit amet, consectetur adipiscing elit. Aliquam erat volutpat. Etiam pharetra eleifend hendrerit.

**REFERENCES**

1. Reference 1
2. Reference 2
3. Reference 3
4. Reference 4
5. Reference 5
6. Reference 6
7. And so on

**APPENDICES**

**Appendix A: Project Schematic**

Put your final project latest schematic here

**Appendix B: Documentation**

Put the documentation (photos) during the making of the project